REMARKS

Claims 62-95 are pending in the present application. Claims 91-95 are new dependent claims. In the Office Action dated January 11, 2005, claims 62-65, 68-75 and 78-82 were rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al. (U.S. Patent No. 5,186,670) and in view of Lee (U.S. Patent No. 5,458,518). Claims 66 and 76 were rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Lee as applied to claim 1 above, and further in view of Jones (U.S. Patent No. 5,869,169). Claims 67, 77 and 83 were rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Lee and Jones as applied to claim 8 above, and further in view of Itoh et al. (U.S. Patent No. 5,793,154). Claims 84-88 and 90 were rejected under 35 U.S.C. 103(a) as being unpatentable over Thoeny et al. (U.S. Patent No. 5,473,222), in view of Doan and Lee (U.S. Patent No. 5,458,518). Claim 89 was rejected under 35 U.S.C. 103(a) as being unpatentable over Thoeny et al. (U.S. Patent No. 5,473,222), Doan and Lee (U.S. Patent No. 5,458,518) and further in view of Jones and Ito as in claim 67.

The disclosed embodiments of the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

One embodiment disclosed in the present application includes a field emission display having a substrate and a plurality of emitters formed on the substrate. Each of the emitters is formed on one of a plurality of emitter conductors that is also a row or a column of the display. The display also includes a porous silicon dioxide dielectric layer formed on the substrate and the columns. The porous silicon dioxide dielectric layer has an opening formed about each of the emitters and has a thickness substantially equal to a height of the emitters above the substrate. The porous silicon dioxide dielectric layer may be formed by oxidation of porous polycrystalline silicon. The display further includes an extraction grid formed substantially in a plane defined by respective tips of the plurality of emitters. The extraction grid has an opening surrounding each tip of a respective one of the emitters. The display additionally includes a cathodoluminescent-coated faceplate having a planar surface formed parallel to and near the plane of tips of the plurality of emitters.

In other embodiments, tips of the emitters are formed from a material having a work function less than four electron volts. The voltage needed in order to drive the emitters, and hence the voltage used to charge and discharge the columns, is proportional to a turn-on

voltage for the emitters. Emitters having reduced turn-on voltage draw less electrical power. As a result, baseplates with emitters having low work function tips are able to form luminous images while dissipating reduced electrical power compared to conventional displays.

The examiner has cited Doan patent, which discloses a field emission device having a silicon dioxide insulating layer formed on a substrate. However, the Doan patent fails to disclose using porous silicon dioxide.

The examiner has also cited the Lee patent. The Lee patent discloses a method of fabricating emitter arrays. One major problem that the Lee patent seeks to solve is the purported lower quality of silicon dioxide layers formed by depositing the silicon dioxide using electron beam evaporation, which are taught to be of lower quality and difficult to control repeatability. (Col. 2, lines 2-7). The Lee patent solves the above problems by forming a porous silicon dioxide layer in the substrate. The porous silicon dioxide layer is formed by etching a silicon substrate 10 to a predetermined depth of about 1 μm by etching in hydrofluoric acid with an electric current applied to form a porous silicon layer 12 in the substrate 10. The porous silicon layer 12 is subsequently oxidized at a temperature of, for example, 1000 °C to form a porous silicon dioxide layer 24. Subsequent steps are directed to integrally forming the emitters in the substrate 10.

The Lee patent clearly teaches away from forming a porous silicon dioxide layer on the substrate 10 using a deposition technique, such as electron beam evaporation, by criticizing the purported difficulty in obtaining consistent process conditions when a silicon dioxide layer is deposited on the substrate 10. Instead, the Lee patent solves this problem by forming the porous silicon dioxide layer in the substrate 10 without resorting to a deposition technique such as electron beam evaporation.

The Yu patent is cited to teach a specific amount of porosity in a silicon dioxide layer.

The Lee patent clearly teaches away from being combined with the Doan patent because the Lee patent requires that the silicon dioxide layer be formed integrally within the substrate as opposed to the Doan patent which teaches forming a silicon dioxide layer on a substrate. If any modification of the Doan patent with the Lee patent is suggested by the cited references, it would be to modify the Doan patent so as to integrally form the silicon dioxide layer 14 in the silicon substrate 11. Combining the Doan and Lee patents would alter one of the Lee patent's fundamental objects. Namely, using a higher quality silicon dioxide layer than can be achieved by forming the silicon dioxide layer on the substrate as in the Doan patent.

Furthermore, the Doan patent teaches away from using a porous silicon dioxide layer because it suggests the use of modifying the chemical composition of the insulating layer 14 and not its structure to presumably control the dielectric properties. (Doan patent, Col. 5, lines 6-14). The Doan patent suggests this because it only suggests using a variety of different compositions (i.e., using silicon dioxide, silicon nitride, or silicon oxynitride) and does not mention altering the structure of the material layer to alter its dielectric properties. Furthermore, neither of the cited references disclose or fairly suggest planarizing the silicon dioxide layer. The Doan patent merely teaches planarizing the focus electrode material as shown in the flow diagram of Figure 8.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Claim 62 recites, in-part, "a porous silicon dioxide layer including respective openings coaxial with the emitter bodies, the porous silicon dioxide layer formed on the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being formed on the substrate and the conductors. Claims depending from claim 62 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, dependent claim 91 recites "wherein the porous silicon dioxide layer has a planarized upper surface and wherein the extraction grid is formed on the planarized upper surface of the porous silicon dioxide layer." Neither of the cited references teaches or suggest a porous silicon dioxide layer having a planarized upper surface.

Claim 68 recites, in-part, "an oxidized porous polysilicon layer formed on the substrate and the conductors." Neither of the cited references, individually or in combination, teaches or suggests the oxidized porous polysilicon layer being formed on the substrate and the conductors. Claims depending from claim 68 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, dependent claim 92 recites "wherein the oxidized porous polysilicon layer has a planarized upper surface and wherein the extraction grid is formed on the planarized upper surface of the oxidized porous polysilicon layer." Neither of the cited references teaches or suggest an oxidized porous polysilicon layer having a planarized upper surface.

Claim 71 recites, in-part, "an oxidized porous polysilicon layer bonded to a surface of the substrate and a surface of the conductors." Neither of the cited references,

individually or in combination, teaches or suggests the oxidized porous polysilicon layer being bonded to a surface of the substrate and a surface of the conductors. Claims depending from claim 71 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, dependent claim 93 recites "wherein the oxidized porous polysilicon layer has a planarized upper surface and wherein the extraction grid is formed on the planarized upper surface of the oxidized porous polysilicon layer." Neither of the cited references teaches or suggest an oxidized porous polysilicon layer having a planarized upper surface.

Claim 78 recites, in-part, "a porous silicon dioxide layer formed on the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three, the porous silicon dioxide layer including respective openings formed about each of the emitters." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being formed on the substrate and the conductors. Claims depending from claim 78 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, dependent claim 94 recites "wherein the porous silicon dioxide layer has a planarized upper surface and wherein the extraction grid is formed on the planarized upper surface of the porous silicon dioxide layer." Neither of the cited references teaches or suggest a porous silicon dioxide layer having a planarized upper surface.

Claim 84 recites, in-part, "a porous silicon dioxide layer including respective openings formed about each of the emitter bodies, the porous silicon dioxide layer formed on the substrate and the conductors, the porous silicon dioxide layer comprising about 22.5 to about 61.5 percent voids and a relative dielectric constant of less than three." Neither of the cited references, individually or in combination, teaches or suggests the porous silicon dioxide being formed on the substrate and the conductors. Claims depending from claim 84 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, dependent claim 95 recites "wherein the porous silicon dioxide layer has a planarized upper surface and wherein the extraction grid is formed on the planarized upper surface of the porous silicon dioxide layer." Neither of the cited references teache or suggest a porous silicon dioxide layer having a planarized upper surface.

All of the claims remaining in the application (62-95) are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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